IN THE SPECIFICATION

Page 1, delete the paragraph and heading inserted at line 7 via the Amendment submitted 10 June 2003 and, in place of that material, insert the following paragraph at line 7 with a heading extending to the left margin:

CROSS-REFERENCE TO RELATED APPLICATION

This is a continuation of U.S. patent application 09/100,384, filed 19 June 1998, now U.S. Patent 6,365,924 B1.

Page 3, amend the paragraph beginning at line 17 as follows:

Fig. 1D shows a top view of SCR 10 constructed using conventional layout techniques. The rectangular shape of p^+ region 20 or n^+ region 22 is known in the art as a finger structure. When an ESD pulse appears across anode terminal 12 and cathode terminal 14, current enters into or departs from p^+ region 20 and n^+ region ~~regions~~ 22 from across only a single edge of each of the fingers, designated in Fig. 1D with solid arrows 40. ~~30.~~ In order to increase the current handling capability--hence to improve the ESD performance of SCR 10--prior art layout techniques add more n^+ fingers in p-type substrate 24 and more p^+ fingers in n-well 26. However, by thus adding more p^+ and n^+ fingers, a significant amount of semiconductor surface area is occupied without a proportional increase in the ESD performance of the resulting structure. This is because, the current flow between each pair of newly added p^+ and n^+ fingers is limited to a component crossing only a single edge of each of the added fingers. It is, therefore, advantageous to develop an ESD layout structure which provides for current flow across more edges of the p^+ and n^+ fingers. ~~finger.~~

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Page 5, amend the paragraph beginning at line 6 as follows:

The ESD protection structure has an anode terminal and a cathode terminal and is composed of five semiconductor regions of alternating conductivity type. In one embodiment, the five regions ~~to~~ form an n-p-n-p-n device. The ESD structure in this

embodiment ~~structure, hence,~~ includes one pnp bipolar transistor and two ~~transistor, two~~ npn bipolar transistors along with ~~and four~~ parasitic resistors.

Page 5, amend the paragraph beginning at line 12 as follows:

When the voltage potential of an ESD pulse appearing across the two terminals of the ESD protection structure exceeds the reverse breakdown voltage of the collector-base junction of the pnp transistor, electron-hole pairs are generated. The holes thus generated flow toward the cathode terminal, forcing the npn transistor whose emitter region is connected to the cathode terminal to turn on. Subsequently, the ESD protection structure enters into a snap-back mode, thereby ~~thereby,~~ to form a low impedance current discharge path between the two terminals to discharge the ESD current. The trigger voltage of the ESD protection structure of the present invention is hence determined by the reverse-breakdown voltage of the collector-base junction of the pnp transistor.

Page 7, amend the paragraph beginning at line 25 as follows:

Fig. 8B shows a cross sectional view of the corner cell of Fig. 8A. ~~10A.~~

Page 8, amend the paragraph beginning at line 13 as follows:

Fig. 11B ~~Fig. 11A~~ shows a top view of a second embodiment of a current-enhanced ESD protection structure, constructed using the corner cell, the center cell and the edge cells of Figs. 8A, 9A and 10A.

Page 10, amend the paragraph beginning at line 26 as follows:

Resistor 132 represents the resistance of the p-base 114 disposed between p^+ region 122 and n-well 116. Resistors 134 and 136 represent the resistances of the n-well region 116. Resistor 134 is located across the base region of transistor 140 and the collector region of transistor 130, ~~130~~ and resistor 136 is located across the base region of transistor 140 and the collector region of transistor 150. Resistor 138 represents the resistance of the p-base 118 disposed between p^+ region 124 and n-well 116.

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Page 11, amend the paragraph beginning at line 27 as follows:

Referring to Fig. 5, when a positive ESD pulse appears across terminals A and K, p-n junction 128 formed between regions 114 and 116 is forward-biased and p-n junction 126 formed between regions 118 and 116 is reverse-biased. When the applied reverse bias across junction 126 exceeds a threshold value, junction 126 enters into a reverse breakdown region thereby generating electron-hole pairs. The holes thus generated accelerate toward p^+ region 124 and are collected by terminal K. As the holes drift toward p^+ region 124, a voltage potential develops across resistor 138 between nodes N1 and N2. Because p^+ region 124 and n^+ region 120 are both connected to terminal K, the voltage across nodes N1 and N2 also appears across nodes ~~nods~~ N1 and N3. When the voltage across nodes N1 and N3 exceeds a certain value, the base-to-emitter junction of npn bipolar transistor 150 is forward-biased thereby turning on npn transistor 150.

Page 12, amend the paragraph beginning at line 29 as follows:

Fig. 6 ~~Fig. 6.~~ shows the current-voltage (I-V) characteristic of a p-n-p-n thyristor 170 of Fig. 5. As the voltage across the two terminals of thyristor 170 increases, the current flow through thyristor 170 increases until the point marked by the I-V coordinates (V_t, I_t), ~~(I_t, V_t),~~ known in the art as the trigger point, is reached. If the voltage across the two terminals increases beyond the trigger voltage, the thyristor enters into a snap-back mode. Thereafter, a low impedance path between the two terminals is formed requiring a much lower voltage to sustain the current flow. Consequently, the voltage across the p-n-p-n device decreases to a new value V_h, commonly known in the art as the holding voltage. The I-V coordinates of the holding point are shown in Fig. 6 as (V_h, I_h). ~~(I_h, V_h).~~ Once the holding voltage is reached, any increase in the voltage across the p-n-p-n device results in a sharp increase in the current through the device. As is seen from Fig. 6, the slope of the I-V characteristic of the device beyond the holding point is very sharp, signifying the high conductance of the device in this deep snap-back region.

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Page 14, amend the paragraph beginning at line 29 as follows:

Fig. 7 shows a top view of the ESD protection structure 100 of the present invention. When an ESD pulse arrives between terminals A and K, current flows between p-base 114 and p-base 118 across section 146 ~~126~~ of n-well 116, as shown by solid arrows 148. ~~130.~~ Therefore, as is seen from Fig. 7, the amount of the current flow is limited to that which crosses only a single edge of each of the p-base regions 114 and 118. In order to increase the amount of current handling capability--hence to increase the ESD protection--prior art techniques add more p-base regions 114 or 118 so as to allow for the addition of more rectangle-shaped p^+ and n^+ regions, which are commonly referred to in the art as finger structures. The conventional technique of adding more p^+ and n^+ fingers, gives rise to a significant increase in the amount of the substrate surface area consumed without a proportional increase in the ESD protection of the resulting structure. Therefore, it is important to develop an ESD protection structure which more efficiently utilizes the substrate surface area to provide a current handling capability that is greater than those known in the prior art.

Page 16, amend the paragraph beginning at line 2 as follows:

From Fig. 8A it is seen that corner cell 300 provides current flow either to or from p^+ region ~~P+ region~~ 124 along the two directions marked by solid arrows 152 and 154. ~~130 and 132.~~ From Fig. 9A, it is seen that center cell 400 provides current flow either to or from p^+ region ~~P+ region~~ 124 along the four directions marked by solid arrows 162, 164, 166 and 168. ~~130, 132, 134 and 136.~~ From Fig. 10A it is seen that edge cell 500 provides current flow either to or from p^+ region ~~P+ region~~ 124 along the two directions marked by solid arrows 172 and 174. ~~130 and 132.~~ As their names imply, corner cell 300, center cell 400 and edge cell 500 are disposed in the corner locations, the center locations and the edge locations of a current-enhanced square-shaped ESD protection structure, in accordance with the present invention.

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Page 16, amend the paragraph beginning at line 18 as follows:

Fig. 11A shows a top view of embodiment 600 of the current-enhanced ESD protection structure of the present invention. Embodiment 600 is composed of four center cells 300, four corner cells 400 and eight edge cells 500. Because of the identical sizes of the cells, embodiment 600 has a square shape. Solid arrows 178 ~~130~~ in Fig. 11A designate the directions in ~~junctions across~~ which currents flow during an ESD pulse. Arrows 178 variously correspond to arrows 152 and 154 in Fig. 8A, arrows 162, 164, 166 and 168 in Fig. 9A, and arrows 172 and 174 in Fig. 10A. As is seen from Fig. 11A, ~~11,~~ depending on the cell types, the current flow between adjacent cells occurs along either two, three or four directions. In contrast, the ESD protection structure of Fig. 7, constructed using conventional layout techniques, provides a current flow between adjacent cells along only one direction. Therefore, ESD protection structure 600 has an enhanced current handling capability and, as such, given identical substrate surface areas, provides a substantially greater degree of ESD protection than does ESD protection structure 100 of Fig. 7.

Page 17, amend the paragraph beginning at line 18 as follows:

As discussed above, the trigger voltage of ESD protection structure 100 of Fig. 5 is determined by the reverse breakdown voltage of junction 126, which typically varies from 15 to 20 volts. The trigger voltage of structure 100 is varied by changing the concentration and the profile of the impurities in n-well 116 and p-base 118 regions. However, it is often not possible to vary the parameters of a CMOS manufacturing process technology in order to change the trigger voltage of an ESD protection structure formed thereby. Therefore, alternative methods of adjusting the trigger voltage of an ESD protection device are needed. ~~is needed~~.

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Page 18, amend the paragraph beginning at line 8 as follows:

Fig. 13 shows a circuit schematic view of ESD protection structure 700 of the present invention. As is seen from Fig. 13, circuit 750 includes branches 780 and 790. Branch 780 includes current source 770 and resistor 756, and branch 790 includes current source 772 and resistor 758. Current source 770 is connected across terminal A and the base terminal of

transistor 150. Resistor 756 is connected across terminal K and the base terminal of transistor 150. (Although not shown in Fig. 12, a line thus connects the base of transistor 150 to a node between resistor 756 and current source 770.) Current source 772 is connected across terminal K and the base terminal of transistor 130. Resistor 758 is connected across terminal A and the base terminal of transistor 130. (Although not shown in Fig. 12, a line thus connects the base of transistor 130 to a node between resistor 758 and current source 772.) The operation of embodiment 700 is discussed next and is best understood by referring to Fig. 12.

Page 20, amend the paragraph beginning at line 15 as follows:

When ~~when~~ a negative voltage/current pulse is applied across terminals A and K, diode 862 enters a reverse breakdown region while diode 860 is forward-biased, forcing transistors 130 and 140 to turn on to thereby trigger structure 800 into a snap-back mode to discharge the current. Consequently, circuit 850 ensures that during an ESD pulse, a current flows either in branch 880--in order to trigger a snap-back between transistors 140 and 150--or in branch 890--in order to trigger a snap-back between transistors 140 and 130--but not in both.

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